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| 09/471,435 | 12/23/1999 | MICHAEL J. MCTAGUE | INTL-0296-US | 7390 |

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| ART UNIT | PAPER NUMBER |
|---|---|
| 2631 | |

DATE MAILED: 08/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/471,435 | MCTAGUE ET AL. | |
| | Examiner | Art Unit | |
| | Khanh Tran | 2631 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *14 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,3-15,17-28 and 30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-15,17-28 and 30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 December 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. The Amendment filed on 06/14/2004 has been entered. Claims 1, 3-15, 17-28, and 30 are pending in this Office action.

### *Response to Arguments*

2. Applicant's arguments with respect to claims 1, 3-15, 17-28, and 30 have been considered but are moot in view of the new ground(s) of rejection.

### *Drawings*

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the claim feature in claims 1, 12 "*a multiplexer to multiplex said lower data rate and control information*"; the claim feature in claim 14 "*multiplexing said serialized data with control information*"; the claim feature in claim 23 "*to multiplex said lower data rate and control information*" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate

prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Claim Objections***

4. Claim 1 is objected to because of the following informalities: in line 5, "said circuit" should be changed to -- said integrated circuit --; in line 7, "rate" should be changed to -- rate data --; in line 9, "said data" should be changed to -- said lower data rate data --. Appropriate correction is required.

5. Claim 4 is objected to because of the following informalities: in line 1, "a analog" should be changed to -- an analog --. Appropriate correction is required.

6. Claim 17 is objected to because of the following informalities: *claim 17 depends on cancelled claim 16*. Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 8 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 8 recites the limitation "a second integrated circuit" in line 1. There is insufficient antecedent basis for this limitation in the claim. *Examiner's comment*: ***a second integrated circuit has been recited two times*** in claims 1 and 8.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1, 3-10, 14-15, 17, 20-23, 25-26, 28 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanekawa et al. U.S. 6,389,063 B1 in view of Yukutake et al. U.S. 6,603,807 B1.

Regarding claim 1, Kanekawa et al. invention is directed to an insulating coupler, or insulating amplifier, or an isolator utilized for electrically separating and insulating between circuits, and a modem utilizing the isolator. In particular, Kanekawa et al. invention utilizes a highly dielectric capacitor that does not break down the device (e.g. a modem in figure 20) and prevents a dangerous voltage from passing the secondary side even if a high voltage is applied.

In column 12 line 1 through column 13 line 35, figure 20 shows a constitution of a modem including a DC blocking switch 204, an analog front end (AFE) 100, and a host 203. The host 203 executes modulation of a sending signal, demodulation of a receiving signal, filtering, and other necessary processes, wherein the host 203 is further realized by a DSP (digital signal processor).

Figure 23 shows a constitution of AFE 100, wherein a clock signal CLK inputted from the host side is transmitted the subscriber line side via an isolating capacitor 2-0 of an isolator 50-0. Control circuits 101 and 102 exchange necessary control information via isolators 2-1 and 2-2 of isolators 50-1 and 50-2.

- As appreciated by one of ordinary skill in the art, AFE 100 is implemented on an integrated circuit. Figure 6 shows the isolating capacitor (isolator) formed on a monolithic integrated circuit. In view of that, it would have been obvious for one of ordinary skill in the art at the time the invention was made that since isolators 50-2, 50-1 and 50-2 could be formed on monolithic integrated circuits and electrically separating and insulating AFE 100, AFE 100 effectively forms two

separate regions, constituting equivalent first and second integrating circuits as claimed in the pending application. The second region on the host side also includes the host 203. Furthermore, with the advance of IC technology, one of ordinary skill in the art will appreciate the recited regions can be formed on integrated circuit.

- The first region connecting to the subscriber line side includes an analog-to-digital converter (ADC) 105 producing data at a relatively higher data rate due to oversampling, a multiplexer 111 for multiplexing the data rate and coded control information from the control circuit 101.
- A second region, connecting to the host side, includes a demultiplexer 112 for demultiplexing the data rate and control information, and a low pass filter and decimator 106 for reducing the data rate. Kanekawa et al. does not show the low pass and decimator 106 coupled to ADC 105 for reducing higher data rate from ADC 105 as claimed in the pending application. Nevertheless, Yukutake et al. discloses a very similar AFE arrangement (see figure 2) in another US patent wherein a decimator 515 coupled to ADC 514 for reducing higher data rate from ADC 514 to transmit the lower data rate data across isolators. Kanekawa et al. and Yukutake et al. teachings are in the same field of endeavor and disclose utilization isolators in a modem. In view of that foregoing reasoning, it would have been obvious for one of ordinary skill in the art at the time the invention was made that Kanekawa et al. AFE can be modified to

implement the low pass and decimator 106 between ADC 105 and MUX 111 for reducing higher data rate data from ADC 105 as claimed in the pending application. Furthermore, the modification will not have any effect on the modem operation.

- As result of the modification, with low pass filter and decimator 106 coupled between ADC 105 and MUX 111, MUX 111 multiplexes lower data rate data and coded control information and transmit lower data rate data and coded control information externally of the first region on the subscriber line side, corresponding to the claimed first integrated circuit, to the region on the host side isolated from the subscriber line side via an isolating capacitor 2-1 of an isolator 50-1. The region on the host side, corresponding to the claimed second integrated circuit, includes a de-multiplexer DE-MUX 112 for de-multiplexing lower data rate data and coded control information as claimed in the pending application.

Regarding claims 3 and 25, with the modification as recited in claim 1, low pass filter and decimator 106 coupled between ADC 105 and MUX 111 in the region on subscriber line side includes a decimation filter as claimed.

Regarding claim 4, with the modification as recited in claim 1, referring to figure 23 above, the first region, corresponding the claimed first integrated circuit as discussed in claim 1, includes an analog pre-filter 104, corresponding to the claimed analog filter,

wherein the analog pre-filter 104 is coupled to ADC 105 in turn coupled to low pass filter and decimator 106 in turn coupled to MUX 111.

Regarding claim 5, referring to figure 23 again, the region on the subscriber line side includes a DE-MUX 113 (de-multiplexer) coupled to a digital-to-analog converter (DAC) 109. Kanekawa et al. does not show a device that increases the data rate of data received by a de-multiplexer as claimed. Nevertheless, using analogous reasoning and motivation as for claim 1 when modifying Kanekawa et al. AFE 100 to couple low pass filter and decimator 106 between ADC 105 and MUX 111, a low pass filter and interpolator 110 in the region on the host side can be modified to locate in the region on the subscriber line side between DE-MUX 113 and a DAC 109 for interpolating a digital signal transmitted from the host side to a signal at the oversampling frequency.

Regarding claims 6 and 26, as recited in claim 5, a low pass filter and interpolator 110 includes an interpolation filter.

Regarding claim 7, referring to figure 23, the region on the subscriber line side further includes a sending amplifier 107, and a receiving amplifier 103, wherein both sending amplifier 107, and receiving amplifier 103 are representative of both a receiver section and a transmitter section as appreciated by one of ordinary skill in the art.

Regarding claim 8, as recited in claim 1, the region on the host side, equivalent to the claimed second integrated circuit, includes a DE-MUX 114, which de-multiplexes a data and coded control information transmitted to the host side. In view of the foregoing, that direction is representative of a receiver section.

Regarding claim 9, as recited in claim 1, the host 203 connected to the analog front end 100 executes modulation of a sending signal, demodulation of a receiving signal, filtering, and other necessary processes, wherein the host 203 is realized by a DSP (digital signal processor). As appreciated by one of ordinary skill in the art that, discrete multi-tone modulation (DMT) is known to be implemented in digital subscriber line (DSL) modem such as the modem illustrated in figure 20. Even though Kanekawa et al. does not expressly teach DMT implemented in the modem of figure 20, one of ordinary skill in the art would have been motivated to implement discrete multi-tone modulation in Kanekawa et al. modem because Kanekawa et al. expresses that the host 203 can be realized by a DSP which is known to implement DMT in the modem.

Regarding claim 10, as recited in claim 1, the host 203 connected to the analog front end 100 executes modulation of a sending signal, demodulation of a receiving signal, filtering, and other necessary processes, wherein the host 203 is realized by a DSP (digital signal processor).

Regarding claim 14, the rejection argument is analogous to that as for claim 1 because claims 1 and 14 are very much similar in scope. Referring to figure 23, on the subscriber line side, a receiving amplifier 103 receives an analog data. ADC 105 converts the analog data into digital format.

Kanekawa et al. does not show the step of decreasing the data rate of said data on the subscriber line side as claimed. Kanekawa et al., however, discloses a low pass filter and decimator 106 for reducing the data rate on the host side. Using analogous reasoning and motivation as for claim 1 to modify Kanekawa et al. AFE 100 to couple low pass filter and decimator 106 between ADC 105 and MUX 111 on the subscriber line side.

With the modification, low pass filter and decimator 106 reduces the data rate data from ADC 105. As appreciated by one of ordinary skill in the art, MUX 111 performs both serialization of data and multiplexing serialized data with coded control information. MUX 111 transmits serialized data with coded control information to the region on host side isolated from the subscriber line side via an isolating capacitor 2-1 of an isolator 50-1.

In the region on host side, a DE-MUX 112 de-multiplexes serialized data with coded control information. As recited in claim 1, the region on the host side including the host 203 is equivalent to the second integrated circuit for the reason as stated in claim 1.

Regarding claim 15, with the modification as recited in claim 1, low pass filter and decimator 106 coupled between ADC 105 and MUX 111 on the subscriber line side performs decimating the digital data.

Regarding claim 17, similar to the reasoning for MUX 111 as recited in claim 14, as appreciated by one of ordinary skill in the art that the demultiplexing process of DE-MUX 112 demultiplexes data into individual data streams. In view of that, the process corresponds to deserializing digital data as claimed.

Regarding claim 20, referring back to figure 23, Kanekawa et al. shows a low pass filter and interpolator 110 for increasing the data rate of the data the region on the host side, corresponding to the second integrated circuit as explained in claim 1. Using analogous reasoning and motivation as for claim 5, it would have been obvious for one of ordinary skill in the art that the low pass filter and interpolator 110 can be modified to couple between DE-MUX 113 and DAC 109 for increasing the data rate of the data as claimed. The region of the subscriber line side receives digital data transmitted from the region on host side.

Regarding claim 21, as recited in claim 20, the low pass filter and interpolator 110 includes an interpolator for interpolating said data.

Regarding claim 22, DAC 109 converts digital data back to an analog format signal.

Regarding claim 23, using analogous reasoning and motivation as for claim 1 due to similar scope, referring back to figure 23, the region on the subscriber line side, equivalent to the claimed first integrated circuit, includes ADC 105, MUX 111 corresponding to the claimed serializer. The low pass filter and decimator 106 for reducing the data rate data, corresponding to the claimed device, is on the region on the host side. However, with the modification and motivation as stated in claim 1, low pass filter and decimator 106 can be modified to couple between ADC 105 and MUX 111 on the region of the subscriber line side.

In view of that, MUX 111 multiplexes lower data rate data and coded control information and transmit lower data rate data and coded control information externally of the first region on the subscriber line side, corresponding to the claimed first integrated circuit, to the region on the host side isolated from the subscriber line side via an isolating capacitor 2-1 of an isolator 50-1. The region on the host side, corresponding to the claimed second integrated circuit, includes a de-multiplexer corresponding to the claimed de-serializer, wherein DEMUX 112 for de-multiplexing lower data rate data and coded control information before transmitting to the host 203.

Regarding claim 28, Kanekawa et al. does not expressly disclose the modem in figure 20 is splitterless. However, the modem in figure 20 suggests a splitterless modem as appreciated by one of ordinary skill in the art.

Regarding claim 30, referring to figure 23 again, lower data rate data is transmitted to the region on host side through low pass filter and decimator 106, and to the region on subscriber line side through low pass filter and interpolator 110. In view of that, lower data rate data is transmitted in two directions as claimed in the pending application.

8. Claims 11, 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanekawa et al. U.S. 6,389,063 B1 and Yukutake et al. U.S. 6,603,807 B1 as applied to claim 9 and further in view of Isaksson et al. U.S. Patent 6,359,926 B1.

Regarding claim 11, since the host 203 executes modulation of a sending signal, demodulation of a receiving signal, filtering, and other necessary processes, the host 203 includes a line decoder as appreciated by one of ordinary skill in the art. Furthermore, DMT system is well known in the art of DSL modem, and is discussed in Isaksson et al. invention. Figure 4 illustrates a DMT transceiver including an analog front end and a digital receiver unit and a digital transmitter unit. Since Kanekawa et al. modem can be modified to implement DMT which always utilizes a Fourier transformer and an inverse Fourier transformer, it would have been obvious for one of ordinary skill

in the art at the time the invention was made that the host 203 can be modified to include a Fourier transformer as that shown in figure 4 of Isaksson et al. invention.

Regarding claim 18, said claim is rejected using analogous argument as for claim 11. The fast Fourier transformer included in the host 203 effectively increases the data rate due to the Fourier transform process as known in the art of DSL modems.

Regarding claim 19, as recited in claim 18, said claim is rejected using analogous argument as for claim 11. In claim 11, the host 203 is modified to implement DMT, resulting utilization of a fast Fourier transformer.

9. Claims 12-13, 24, 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanekawa et al. U.S. 6,389,063 B1 and Yukutake et al. U.S. 6,603,807 B1 as applied to claim 1 and further in view of Isaksson et al. U.S. Patent 6,359,926 B1.

Regarding claim 12, claim 1 rejection argument addresses all the limitations of claim 12, except the limitation encompassing a second integrated circuit as set forth in claim 12. As recited in claim 1, the host 203 executes modulation of a sending signal, demodulation of a receiving signal, filtering, and other necessary processes, the host 203 includes a line encoder as appreciated by one of ordinary skill in the art. Furthermore, using analogous reasoning and motivation as for claim 11, DMT system is well known in the art of DSL modem, and is discussed in Isaksson et al. invention. Since Kanekawa et al. modem can be modified to implement DMT, it would have been

obvious for one of ordinary skill in the art at the time the invention was made that the host 203 can be modified to further include a scaling and inverse fast Fourier transformer (IFFT) as shown in figure 4 of Isaksson et al. invention.

Regarding claims 13 and 27, as recited in claim 12, the host 203 also includes a scaling and inverse fast Fourier transformer (IFFT) similar to that shown in figure 4 of Isaksson et al. invention.

Regarding claim 24, claims 13 and 24 are very similar in scope. Claim 24 is rejected on the same ground as claim 13. The modulating circuit for decreasing the data rate of digital data in claim 24 corresponds to an inverse fast Fourier Transformer which has been rejected as stated in claim 13. The serializer on the second integrated circuit in claim 24 corresponds to a serializer in claim 12 on which claim 13 depends.

However, claim 13 does not address the first integrated circuit including a de-serializer as set forth in claim 24. The de-serializer as set forth in claim 24 has been addressed in the rejection of claim 5 wherein DE-MUX 113 performs equivalent function of a de-serializer.

Furthermore, as recited in claim 5, referring to figure 23 again, the region on the subscriber line side includes a DE-MUX 113 (de-multiplexer) coupled to a digital-to-analog converter (DAC) 109. Kanekawa et al. does not show a low pass filter and interpolator 110 in the region on the subscriber line side, corresponding

to the claimed device that increases the data rate of data received by a de-multiplexer as claimed. Nevertheless, using analogous reasoning and motivation as for claim 1 when modifying Kanekawa et al. AFE 100 to couple low pass filter and decimator 106 between ADC 105 and MUX 111, a low pass filter and interpolator 110 in the region on the host side can be modified to locate in the region on the subscriber line side between DE-MUX 113 and a DAC 109 for interpolating a digital signal transmitted from the host side to a signal at the oversampling frequency.

***Conclusion***

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Camagna et al. U.S. Patent 6,707,868 B1 discloses "Apparatus for Recovering Timing of a Digital Signal for a Tranceiver".

Girardeau, Jr. et al. U.S. Patent 6,535,565 B1 discloses "Receiver Rate Converter Phase Calculation Apparatus and Method".

Belloc et al. U.S. Patent 5,038,365 discloses "Modem Having a Software-Adapted Modulation Rate".

Lindsey et al. U.S. Patent 6,226,296 B1 discloses "Metropolitan Area Network Switching System and Method of Operation Thereof".

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Tran whose telephone number is 703-305-2384. The examiner can normally be reached on Tuesday - Friday from 08:00 AM - 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 703-306-3034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KCT